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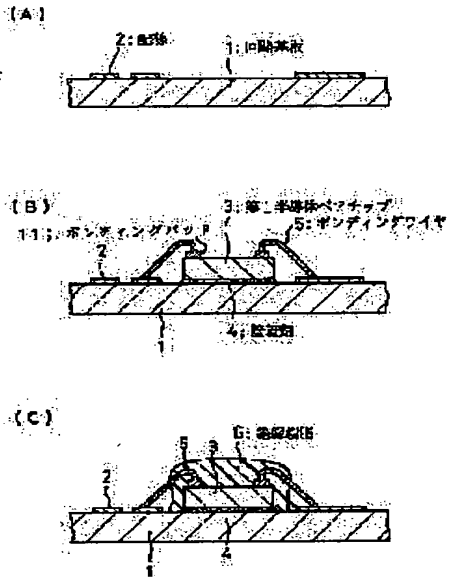
(54) HYBRID IC AND ITS MANUFACTURE

(57)Abstract:

PURPOSE: To provide a high-density bare-chip mounting method whose application range is wide and which can be executed easily when a plurality of semiconductor bare chips are built in a hybrid IC.

CONSTITUTION: A first semiconductor bare chip 3 is fixed and bonded to a circuit board 1. A wire bonding operation is performed. The first semiconductor bare chip 3 is coated with a liquid insulating resin 6 up to a height at which at least bonding wires 5 are covered. A second semiconductor bare chip is placed on it. After that, the insulating resin 6 is hardened. A wire bonding operation is performed. Lastly, the semiconductor bare chip 3 and all the bonding wires 5 are sealed with a sealing resin. Thereby, a plurality of semiconductor bare chips can be mounted on one face of the circuit board easily, in a multistage manner and at high density without taking into consideration the relationship between an upper size and a lower size.



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CLAIMS

[Claim(s)]
[Claim 1] Circuit connection of the 1st semi-conductor bare chip is made. a circuit board top -- the 1st semi-conductor bare chip -- fixing -- a metal thin line -- this circuit board -- this -- next -- this -- the liquefied insulation resin hardened by after treatment on the principal plane which the 1st semi-conductor bare chip exposed at least -- this -- up to the maximum height part of this metal thin line on the 1st semi-conductor bare chip -- a wrap, while discharge and said insulating resin have been in the condition of not hardening, like Place the 2nd semi-conductor bare chip on said insulating resin, and circuit connection of said circuit board and said 2nd semi-conductor bare chip is made with a metal thin line after that. final -- this -- the manufacture approach of the hybrid IC characterized by what the 1st and 2nd semi-conductor bare chip and said whole metal thin line for circuit connection are closed by insulating resin, and a semiconductor chip is built in for.
[Claim 2] The manufacture approach of the hybrid IC according to claim 1 characterized by making circuit connection of said circuit board and said 2nd semi-conductor bare chip with said metal thin line after stiffening said insulating resin.
[Claim 3] The manufacture approach of the hybrid IC according to claim 1 characterized by adding the process which forms the spacer which consists of an insulator on said 1st semi-conductor bare chip in the phase before carrying out the regurgitation of said liquefied insulation resin after making circuit connection of said circuit board and said 1st semi-conductor bare chip with said metal thin line.
[Claim 4] The manufacture approach of the hybrid IC according to claim 1 characterized by circuit connection accomplishing said circuit board and said semi-conductor bare chip at least by wirebonding of a gold streak by which the insulating resin coat was carried out in said 1st semi-conductor bare chip.
[Claim 5] It is the manufacture approach of the hybrid IC which accumulates two or more semi-conductor bare chips, and changes on the circuit board. Fix the semi-conductor bare chip of the 1st layer, and circuit connection of the semi-conductor bare chip of this circuit board and this 1st layer is made with a metal thin line. In case further two or more semi-conductor bare chips are accumulated on the semi-conductor bare chip of said 1st layer After making circuit connection of the semi-conductor bare chip of the layer of the already arranged bottom with this circuit board with a metal thin line Insulating resin so that it may cover at least on the semi-conductor bare chip of the layer of said bottom to the maximum height part of said metal thin line of the semi-conductor bare chip of the layer of said bottom Discharge, Place the semi-conductor bare chip of an upper layer on said insulating resin, and make circuit connection of the semi-conductor bare chip of said circuit board and the layer of an above upside with a metal thin line. The manufacture approach of the hybrid IC characterized by the thing close two or more semi-conductor bare chips by which repeat a process successively, and carry out the laminating of two or more semi-conductor bare chips, and the laminating was carried out to the last, and said whole metal thin line for circuit connection by insulating resin, and it is made to build in a semiconductor chip for.
[Claim 6] The manufacture approach of the hybrid IC according to claim 5 characterized by said insulating resin breathed out on the semi-conductor bare chip of a lower layer arranging the semi-conductor bare chip of the layer of said upside on this insulating resin in that in the condition of not hardening.
[Claim 7] The manufacture approach of the hybrid IC according to claim 5 characterized by forming the

spacer which consists of an insulator before the regurgitation of said insulating resin on the semi-conductor bare chip of the layer of said bottom after making circuit connection of the semi-conductor bare chip of said circuit board and layer of said bottom with said metal thin line.
[Claim 8] The manufacture approach of the hybrid IC according to claim 5 characterized by circuit connection accomplishing the semi-conductor bare chip of the circuit board and a lower layer at least by wirebonding of a gold streak by which the insulating resin coat was carried out in at least 1 of the semi-conductor bare chip of a lower layer.
[Claim 9] The 1st semi-conductor bare chip which fixed on the circuit board and was connected with this circuit board with the metal thin line, this -- a 1st semi-conductor bare chip top -- at least -- this -- up to the maximum height part of this metal thin line on the 1st semi-conductor bare chip -- a wrap -- with the insulating resin breathed out like The hybrid IC which is placed on this insulating resin, is equipped with the 2nd semi-conductor bare chip which made circuit connection with said circuit board with a metal thin line, closes the said 1st and 2nd semi-conductor bare chip and said whole metal thin line for circuit connection by insulating resin, and changes.
[Claim 10] The hybrid IC according to claim 9 characterized by arranging the spacer which consists of an insulator on said 1st semi-conductor bare chip.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the hybrid IC which builds in two or more semiconductor chips especially, and its manufacture approach about a hybrid IC and its manufacture approach.
[0002]
[Description of the Prior Art] When the conventional hybrid IC builds two or more semi-conductor bare chips in high density, as are shown in drawing 5 , and the 1st and 2nd semi-conductor bare chip 3 and 7 is ****(ed) to both sides of the circuit board 1, respectively or it is shown in drawing 6 , the method of accumulating two or more steps of 1st and 2nd semi-conductor bare chip 3 and 7, and ****(ing) it on one side, is taken.
[0003] The 2nd semi-conductor bare chip 7 is directly pasted up with adhesives 4 on the 1st semi-conductor bare chip 3 on the circuit board 1, and wirebonding of the 1st and 2nd semi-conductor bare chips 3 and 7 and circuit board 1 is carried out after that when accumulating two or more steps of semi-conductor bare chips on one side, for example, so that it may be indicated by JP,62-81721,A. That is, in the semiconductor device of said JP,62-81721,A, those bonding pads 11 and wiring 2 of the circuit board 1 are electrically connected to ****** for the 1st and 2nd semi-conductor bare chip 3 and 7 by the bonding wire 5 after ******.
[0004]
[Problem(s) to be Solved by the Invention] in said conventional hybrid IC, as shown in drawing 5 , when

it is going to **** a semi-conductor bare chip to both sides of the circuit board 1, after performing wirebonding, such as adhesion of a semi-conductor bare chip and a gold streak, at least, on the other hand, one side must be boiled, and must be set, the same activity must be done, and the stage which avoided the projection by the side of a rear face is needed at the time of the activity of other sides.
[0005] For this reason, in wirebonding, it was difficult to acquire the uniform temperature distribution at the time of immobilization of the circuit board, or heating, and there was a difficult thing in that manufacture.
[0006] moreover, as shown in drawing 6 , in accumulating two or more steps of semi-conductor bare chips on one side of the circuit board 1 On the 1st [of the circuit board 1] semi-conductor bare chip 3, preferably The laminating of the 2nd semi-conductor bare chip 7 is carried out through the layer of the about 50-micrometer thin insulating adhesives 4. The magnitude of the 2nd semi-conductor bare chip 7 There is size restriction that it must be the thing of the magnitude within the limits settled in the field inside the part (boundary region of the chip with which a bonding pad 11 is arranged) into which wirebonding of the 1st semi-conductor bare chip 3 is performed.
[0007] For this reason, in the case of the approach shown in drawing 6 , there was a trouble that the degree of freedom of a design became small for the above-mentioned limit.
[0008] Therefore, when said trouble is canceled and it builds two or more semi-conductor bare chips in a hybrid IC, applicability of this invention is wide, and it aims at offering the mounting approach of the high density bare chip which can be carried out easily. Moreover, this invention cancels a limit of the degree of freedom of a design, and aims at offering the hybrid IC in which high density assembly is possible.
[0009]
[Means for Solving the Problem] In order to attain said object, the manufacture approach of the hybrid IC of this invention Circuit connection of the 1st semi-conductor bare chip is made. a circuit board top -- the 1st semi-conductor bare chip -- fixing -- a metal thin line -- this circuit board -- this -- next -- this -- the liquefied insulation resin hardened by after treatment on the principal plane which the 1st semi-conductor bare chip exposed at least -- this -- up to the maximum height part of this metal thin line on the 1st semi-conductor bare chip -- a wrap, while discharge and said insulating resin have been in the condition of not hardening, like Place the 2nd semi-conductor bare chip on said insulating resin, and circuit connection of said circuit board and said 2nd semi-conductor bare chip is made with a metal thin line after that. final -- this -- it is characterized by what the 1st and 2nd semi-conductor bare chip and said whole metal thin line for circuit connection are closed by insulating resin, and a semiconductor chip is built in for.
[0010] In the manufacture approach of the hybrid IC of this invention, preferably, after stiffening said insulating resin, it is characterized by making circuit connection of said circuit board and said 2nd semi-conductor bare chip with said metal thin line.
[0011] Moreover, in the manufacture approach of the hybrid IC of this invention, after making circuit connection of said circuit board and said 1st semi-conductor bare chip with said metal thin line, it is the phase before carrying out the regurgitation of said liquefied insulation resin, and is characterize by adding the process which forms the spacer which consists of an insulator on said 1st semi-conductor bare chip.
[0012] Furthermore, in the manufacture approach of the hybrid IC of this invention, it is characterized by circuit connection accomplishing [in / at least / said 1st semi-conductor bare chip] said circuit board and semi-conductor bare chip by wirebonding of a gold streak by which the insulating resin coat was carried out.
[0013] And it is the manufacture approach of the hybrid IC which accumulates two or more semi-conductor bare chips, and changes on the circuit board in this invention. Fix the semi-conductor bare chip of the 1st layer, and circuit connection of the semi-conductor bare chip of this circuit board and this 1st layer is made with a metal thin line. In case further two or more semi-conductor bare chips are accumulated on the semi-conductor bare chip of said 1st layer After making circuit connection of the semi-conductor bare chip of the layer of the already arranged bottom with this circuit board with a

metal thin line Insulating resin so that it may cover at least on the semi-conductor bare chip of the layer of said bottom to the maximum height part of said metal thin line of the semi-conductor bare chip of the layer of said bottom Discharge, Place the semi-conductor bare chip of an upper layer on said insulating resin, and make circuit connection of the semi-conductor bare chip of said circuit board and the layer of an above upside with a metal thin line. The manufacture approach of the hybrid IC characterized by the thing close two or more semi-conductor bare chips by which repeat a process successively, and carry out the laminating of two or more semi-conductor bare chips, and the laminating was carried out to the last, and said whole metal thin line for circuit connection by insulating resin, and it is made to build in a semiconductor chip for is offered.

[0014] In the manufacture approach of the hybrid IC of this invention, it is characterized by said insulating resin breathed out on the semi-conductor bare chip of a lower layer arranging the semi-conductor bare chip of the layer of said upside on this insulating resin in the condition of not hardening, preferably.

[0015] In the manufacture approach of the hybrid IC of this invention, preferably, after making circuit connection of the semi-conductor bare chip of said circuit board and layer of said bottom with said metal thin line, it is characterized by forming the spacer which consists of an insulator before the regurgitation of said insulating resin on the semi-conductor bare chip of the layer of said bottom. It is characterized by furthermore circuit connection accomplishing [in / at least / at least 1 of the semi-conductor bare chip of a lower layer] the semi-conductor bare chip of the circuit board and a lower layer in this invention by wirebonding of a gold streak by which the insulating resin coat was carried out.

[0016] Moreover, the 1st semi-conductor bare chip which this invention fixed on the circuit board and was connected with this circuit board with the metal thin line, this -- a 1st semi-conductor bare chip top -- at least -- this -- up to the maximum height part of this metal thin line on the 1st semi-conductor bare chip -- a wrap -- with the insulating resin breathed out like It is placed on this insulating resin, and has the 2nd semi-conductor bare chip which made circuit connection with said circuit board with a metal thin line, and the hybrid IC which closes the said 1st and 2nd semi-conductor bare chip and this whole circuit connection metal thin line by insulating resin, and changes is offered.

[0017] In the hybrid IC of this invention, it is characterized by arranging preferably the spacer which consists of an insulator on said 1st semi-conductor bare chip.

[0018]

[Function] By according to this invention, having prepared the insulating layer by insulating resin etc. more highly than wire height on the semi-conductor bare chip with which wirebonding of [on the circuit board] was carried out, and having arranged another semi-conductor bare chip on it Since the constraint on a dimension does not exist about the up-and-down semi-conductor bare chip with which manufacture is easy with a bare chip and a laminating is carried out farther [since two or more semi-conductor bare chips can be carried in the one side side of the circuit board] than the case where it **** to both sides of the circuit board, Constraint is not imposed on a degree of freedom of a design like said conventional example that an upper semi-conductor bare chip must be smaller than a lower semi-conductor bare chip by size predetermined in a flat-surface dimension.

[0019] Moreover, according to this invention, the rear face of an upper semi-conductor bare chip and the bonding wire of a lower semi-conductor bare chip are mutually insulated electrically by the insulating resin layer inserted between them about the semi-conductor bare chip of the upper and lower sides by which a laminating is carried out. And in order to secure isolation with the rear face of an upper semi-conductor bare chip, and the bonding wire of a lower semi-conductor bare chip in this invention and to ensure an electric insulation, a spacer is arranged at a lower semi-conductor bare chip.

[0020]

[Example] With reference to a drawing, the example of this invention is explained below.

[0021]

[Example 1] Drawing 1 and drawing 2 show the cross-section structure of the semi-conductor bare chip loading part of the hybrid IC of one example of this invention in order of a process. In addition, for the reason of drawing creation, a production process covers drawing 1 and drawing 2 , and is only shown.

[0022] As shown with reference to drawing 1 at drawing 1 (B) on the circuit board 1 to which predetermined wiring 2 was given (refer to drawing 1 (A)), the 1st semi-conductor bare chip 3 is fixed with adhesives 4 to circuit board top 1, and the bonding pad 11 of the 1st semi-conductor bare chip 3 and the predetermined wiring 2 of the circuit board 1 are mutually connected by the bonding wire 5 using the wirebonding method.
[0023] As for a bonding wire 5, the gold streak of the diameter of 25 micrometers - 30 micrometer is usually used.
[0024] Next, as shown in drawing 1 (C), the regurgitation of the insulating resin 6 is carried out on the 1st semi-conductor bare chip 3. Insulating resin 6 is used as the liquefied resin hardened by after treatment, and preferably, it consists of an epoxy resin of a heat-curing mold etc., and what sagging does not generate greatly is used after having and carrying out the regurgitation of suitable viscosity and the thixotropy until it hardens. And insulating resin 6 is desirable and the thing of viscosity 100 - 200 Pa-s, and the TI values (CHIKUSO ratio) 2-3 is used.
[0025] With reference to drawing 1 (C), the regurgitation of insulating resin 6 is performed so that the bottom of the 2nd semi-conductor bare chip 7 behind carried on it may be filled up with insulating resin 6, and so that it may become higher than the bonding wire 5 given previously.
[0026] For example, if the wire loop-formation height from the chip side of the 1st semi-conductor bare chip 3 is 200 micrometers, 300 micrometers will be heaped up from the chip side of the 1st semi-conductor bare chip 3, and it will apply to the bigger range than the 2nd semi-conductor bare chip size carried upwards.
[0027] Next, as shown in drawing 2 (D), the 2nd semi-conductor bare chip 7 is carried on the breathed-out insulating resin 6, and hardening processing of insulating resin 6 is performed.
[0028] With un-hardening insulating resin 6, the level nature of the chip side of the 2nd semi-conductor bare chip 7 can secure easily by carrying the 2nd semi-conductor bare chip 7.
[0029] Moreover, it is desirable when performing height control secures distance with the lower bonding wire 5 at the time of the 2nd semi-conductor bare chip loading.
[0030] Then, as shown in drawing 2 (E), the 2nd semi-conductor bare chip 7 and the circuit board 1 are connected by the bonding wire 5, and all the 1st and 2nd semi-conductor bare chips 3 and 7 and bonding wires 5 are eventually closed by closure resin 8.
[0031] The bonding wire 5 on the 1st semi-conductor bare chip 3, and the rear face of the 2nd semi-conductor bare chip 7 On electrical characteristics, although it must insulate mutually, as the process of drawing 1 (C) explained By performing adjustment of the description of the insulating resin breathed out, an amount, and semi-conductor bare chip loading conditions, the layer of insulating resin 6 is inserted between the bonding wire 5 on the 1st semi-conductor bare chip 3, and the rear face of the 2nd semi-conductor bare chip 7, it is isolated mutually and these are insulated electrically.
[0032]
[Example 2] Next, another example of this invention is explained below.
[0033] When it is difficult to adopt in said 1st example under the effect which gives the insulating resin 6 of desired description to an electrical property and dependability, Or by the case where the optimal manufacturing installation cannot be used on a production process etc. When it is difficult to stabilize and prepare the layer of insulating resin 6 between the bonding wire 5 on the 1st bare chip 3, and the 2nd semi-conductor bare chip 7, the another manufacture approach shown in drawing 3 or drawing 4 is taken.
[0034] After performing wirebonding of the 1st semi-conductor bare chip 3 in this example with reference to drawing 3 , before carrying out the regurgitation of the insulating resin 6, the insulating spacer 9 which has the height which is sufficient for avoiding certainly contact to the bonding wire 5 on the 1st semi-conductor bare chip 3 with the insulating adhesives 4 is made to fix on the 1st semi-conductor bare chip 3. And after making a spacer 9 fix, the regurgitation of the insulating resin 6 is carried out like said 1st example.
[0035] When forming the insulating spacer 9 on the 1st semi-conductor bare chip 3 according to this example, and the selection width of face is eased and a spacer 9 intervenes further rather than said 1st

example about descriptions, such as viscosity of insulating resin 6, and thixotropy In case the 2nd semi-conductor bare chip 7 is placed on insulating resin 6, control of the pressure which joins insulating resin 6 is simplified, and height control at the time of loading of the 2nd semi-conductor bare chip 7 is also easy-ized. Furthermore, since isolation with the rear face of the 1st semi-conductor bare chip 3 and a bonding wire 5 is decided and secured by the spacer 9, it is supposed that it is possible to aim at improvement in dependability and the yield.

[0036]

[Example 3] Or as another example of this invention, as shown in drawing 4 R> 4, the pre-insulation bonding wire 10 to which pre-insulation was performed as a bonding wire on the 1st semi-conductor bare chip 3 is used in the case of wirebonding of the 1st semi-conductor bare chip 3 used as a lower layer. As a pre-insulation bonding wire, there are an SL wire by the Tanaka electronic industry company, a W type wire by the Japanese micro metal company, etc., for example.

[0037] As mentioned above, although each above-mentioned example explained to the example the semi-conductor bare chip by which the laminating was carried out to two steps in this invention, the manufacture approach of the hybrid IC concerning this invention can be similarly used, when accumulating three or more steps of semi-conductor bare chips.

[0038] When accumulating three or more steps of semi-conductor bare chips, the insulating resin breathed out on the semi-conductor bare chip of a lower layer continues [and] being in the condition of not hardening. After it places the semi-conductor bare chip of an upper layer and insulating resin hardens, may be made to perform wirebonding with the circuit board, and Or while insulating resin has been in the condition of not hardening, wirebonding of the semi-conductor bare chip of an upper layer and the circuit board is performed, and hardening of the insulating resin of each class may be made to advance on a simultaneous target according to the description of insulating resin etc. In this case, a production process is shortened.

[0039] As mentioned above, although this invention was based and explained to various modes, this invention is not limited only to the above-mentioned example, and contains the various modes according to the principle of this invention.

[0040]

[Effect of the Invention] As explained above, according to the manufacture approach of the hybrid IC of this invention By having prepared the insulating layer by insulating resin etc. more highly than wire height on the semi-conductor bare chip with which wirebonding of [on the circuit board] was carried out, and having arranged another semi-conductor bare chip on it Since it is supposed that manufacture is easier than the case where it **** to both sides since two or more semi-conductor bare chips can be built in the one side side of the circuit board and the constraint on the dimension of an up-and-down semi-conductor bare chip does not exist, While the degree of freedom of a design is extended and applicability is expanded, two or more steps of high density assembly is easy-ized, and it has the effectiveness of improving the yield.

[0041] According to this invention, the rear face of a semi-conductor bare chip and the bonding wire of a lower layer semi-conductor bare chip are certainly insulated mutually electrically by the insulating resin layer inserted between them. And since according to this invention the breathed-out insulating resin is placed while in the condition of not hardening, and a semi-conductor bare chip is placed on it, the level nature of a chip side is secured easily.

[0042] According to the manufacture approach of the hybrid IC of this invention, for example moreover, for reasons of manufacture etc. When the positive insulation by the insulating resin layer of the rear face of a semi-conductor bare chip and the bonding wire of a lower layer semi-conductor bare chip is made difficult, Since two or more semi-conductor bare chips can be built in the one side side of the circuit board by forming the spacer which consists of an insulator before the regurgitation of insulating resin on a lower layer semi-conductor bare chip, Manufacture is easier than the case where it **** to both sides, and since the constraint on the dimension of an up-and-down semi-conductor bare chip does not exist, the degree of freedom of a design spreads and it has the effectiveness that the range of application is made greatly. When a spacer is furthermore formed, while height control in a lower layer

semi-conductor bare chip and the upper semi-conductor bare chip is made easy, let an electric insulating layer be a positive thing.
[0043] Furthermore, according to the manufacture approach of the hybrid IC of this invention, it has the effectiveness of securing an electric insulating layer, also by using a pre-insulation bonding wire as a bonding wire of the semi-conductor bare chip by the side of a lower layer.
[0044] And when carrying out high density assembly to multistage, while according to the configuration of the hybrid IC of this invention constraint of the degree of freedom of the design on the dimension which existed conventionally is canceled and applicability is expanded, the electric insulation of each class and a bonding wire is secured, a production process is easy-ized, and the yield is raised.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] (A) - (C) is the sectional view having shown the production process of one example of this invention in order.
[Drawing 2] (D) - (E) is the sectional view having shown in order the production process (process which follows drawing 1) of one example of this invention.
[Drawing 3] It is the sectional view showing the 2nd example of this invention.
[Drawing 4] It is the sectional view showing the 2nd example of this invention.
[Drawing 5] It is the sectional view showing the configuration of the conventional example.
[Drawing 6] It is the sectional view showing the configuration of another conventional example.
[Description of Notations]
1 Circuit Board
3 1st Semi-conductor Bare Chip
5 Bonding Wire
6 Insulating Resin
7 2nd Semi-conductor Bare Chip
9 Spacer
10 Pre-insulation Bonding Wire
11 Bonding Pad

[Translation done.]

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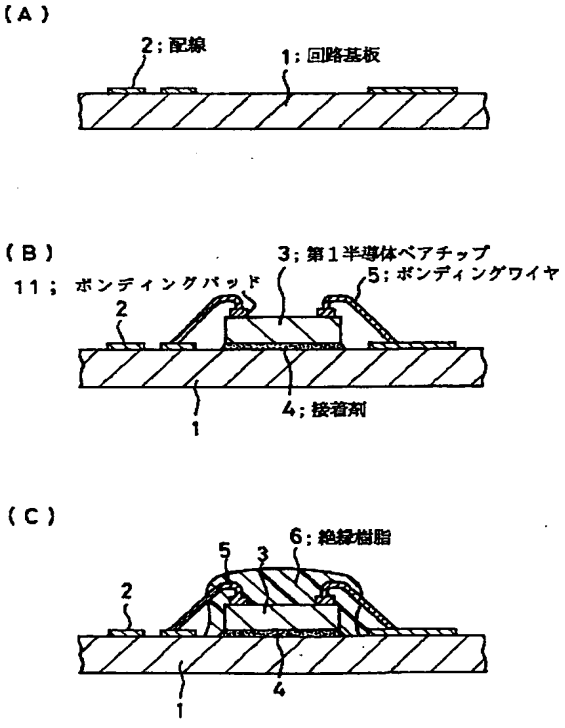
(54)【発明の名称】　ハイブリッドＩＣ及びその製造方法

(57)【要約】

【目的】ハイブリッドＩＣに複数の半導体ベアチップを内蔵する場合に、適用範囲が広く、容易に実施できる高密度なベアチップ実装方法を提供する。

【構成】回路基板(1)上に第１半導体ベアチップ(3)を固着し、ワイヤボンディングを行なった後、液状の絶縁樹脂(6)を第１半導体ベアチップ(3)上に少なくともボンディングワイヤ(5)が覆われる高さまで塗布し、その上に第２半導体ベアチップ(7)を置載し、その後絶縁樹脂(6)を硬化させ、ワイヤボンディングを行なって、最後に半導体ベアチップ(3、7)とボンディングワイヤ(5)の全てを封止樹脂(8)で封止する。これにより、回路基板の片面に複数の半導体ベアチップを、上下の大きさの関係を考慮せずに、容易に多段に高密度実装できる。



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【特許請求の範囲】

【請求項１】回路基板上に第１の半導体ベアチップを固着し、金属細線にて該回路基板と該第１の半導体ベアチップを回路接続し、

次に、該第１の半導体ベアチップの露出した主面上に、後処理によって硬化する液状絶縁樹脂を、少なくとも該第１の半導体ベアチップ上の該金属細線の最大高さ部分まで覆うように吐出し、

前記絶縁樹脂が未硬化状態のまま、第２の半導体ベアチップを前記絶縁樹脂上に置き、

その後、金属細線にて前記回路基板と前記第２の半導体ベアチップを回路接続し、

最終的に該第１、第２の半導体ベアチップと回路接続用の前記金属細線の全体を絶縁樹脂で封止して半導体チップを内蔵する、

ことを特徴とするハイブリッドＩＣの製造方法。

【請求項２】前記絶縁樹脂を硬化させた後に、前記金属細線にて前記回路基板と前記第２の半導体ベアチップを回路接続することを特徴とする請求項１記載のハイブリッドＩＣの製造方法。

【請求項３】前記回路基板と前記第１の半導体ベアチップを前記金属細線で回路接続した後、前記液状絶縁樹脂を吐出する前の段階で、絶縁体から成るスペーサを前記第１の半導体ベアチップ上に形成する工程が追加されたことを特徴とする請求項１記載のハイブリッドＩＣの製造方法。

【請求項４】前記回路基板と前記半導体ベアチップを回路接続が、少なくとも前記第１の半導体ベアチップにおいては、絶縁樹脂被覆された金線のワイヤボンディングにより成されることを特徴とする請求項１記載のハイブリッドＩＣの製造方法。

【請求項５】回路基板上に複数の半導体ベアチップを積み重ねて成るハイブリッドＩＣの製造方法であって、

第１層の半導体ベアチップを固着し、金属細線にて該回路基板と該第１の層の半導体ベアチップを回路接続し、

前記第１の層の半導体ベアチップ上にさらに複数の半導体ベアチップを積み重ねる際に、

すでに配置された下側の層の半導体ベアチップを金属細線にて該回路基板と回路接続した後に、前記下側の層の半導体ベアチップ上に絶縁樹脂を、少なくとも前記下側の層の半導体ベアチップの前記金属細線の最大高さ部分まで覆うように吐出し、

前記絶縁樹脂上に上側の層の半導体ベアチップを置き、

金属細線にて前記回路基板と前記の上側の層の半導体ベアチップを回路接続する、工程を順次繰り返して複数の半導体ベアチップを積層していき、

最後に積層された複数の半導体ベアチップと回路接続用の前記金属細線の全体を絶縁樹脂で封止して半導体チップを内蔵するようにする、

ことを特徴とするハイブリッドＩＣの製造方法。

2

【請求項６】下側の層の半導体ベアチップ上に吐出された前記絶縁樹脂が未硬化の状態のにおいて前記上側の層の半導体ベアチップを該絶縁樹脂上に配置するようにしたことを特徴とする請求項５記載のハイブリッドＩＣの製造方法。

【請求項７】前記回路基板と前記下側の層の半導体ベアチップを前記金属細線で回路接続した後、前記絶縁樹脂の吐出以前に、絶縁体から成るスペーサを前記下側の層の半導体ベアチップ上に形成することを特徴とする請求項５記載のハイブリッドＩＣの製造方法。

【請求項８】回路基板と下側の層の半導体ベアチップを回路接続が、少なくとも下側の層の半導体ベアチップの少なくとも一においては、絶縁樹脂被覆された金線のワイヤボンディングにより成されることを特徴とする請求項５記載のハイブリッドＩＣの製造方法。

【請求項９】回路基板上に固着され、金属細線にて該回路基板と接続された第１の半導体ベアチップと、

該第１の半導体ベアチップ上に少なくとも該第１の半導体ベアチップ上の該金属細線の最大高さ部分まで覆うように吐出された絶縁樹脂と、

該絶縁樹脂上に置かれ、金属細線にて前記回路基板と回路接続した第２の半導体ベアチップと、

を備え、

前記第１、第２の半導体ベアチップと回路接続用の前記金属細線の全体を絶縁樹脂で封止して成るハイブリッドＩＣ。

【請求項１０】前記第１の半導体ベアチップ上に絶縁体から成るスペーサが配設されたことを特徴とする請求項９記載のハイブリッドＩＣ。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、ハイブリッドＩＣ及びその製造方法に関し、特に複数の半導体チップを内蔵するハイブリッドＩＣ及びその製造方法に関する。

【０００２】

【従来の技術】従来のハイブリッドＩＣは、複数の半導体ベアチップを高密度に内蔵する場合、例えば図５に示すように、回路基板１の両面にそれぞれ第１、第２の半導体ベアチップ３、７を置載するか、或いは、図６に示すように、片面に第１、第２の半導体ベアチップ３、７を複数段積み重ねて置載する方法がとられる。

【０００３】片面に半導体ベアチップを複数段積み重ねる場合、例えば特開昭62－81721号公報に開示されるように、回路基板１上の第１の半導体ベアチップ３の上に第２の半導体ベアチップ７を接着剤４により直接接着して、その後、第１、第２の半導体ベアチップ３、７と回路基板１とをワイヤボンディングしている。すなわち、前記特開昭62－81721号公報の半導体装置では、第１、第２の半導体ベアチップ３、７を縦積みに搭載た後に、それらのボンディングパッド11と回路基板１の配線２と

をボンディングワイヤ５により電気的に接続してる。

【０００４】

【発明が解決しようとする課題】前記従来のハイブリッドＩＣでは、図５に示すように、回路基板１の両面に半導体ベアチップを置載しようとした場合には、片面を少なくとも半導体ベアチップの接着、金線等のワイヤボンディングを行なった後、他面において同様の作業を行なわなければならず、他面の作業時には、裏面側の突起を回避したステージ等が必要とされる。

【０００５】このためワイヤボンディングにおいては、回路基板の固定や加熱時の均一な温度分布を得ることが難しく、その製造には困難なことがあった。

【０００６】また、図６に示すように、回路基板１の片面に半導体ベアチップを複数段積み重ねる場合には、回路基板１の第１の半導体ベアチップ３上に、好ましくは、50μｍ程度の薄い絶縁性接着剤４の層を介して第２の半導体ベアチップ７が積層されており、第２の半導体ベアチップ７の大きさは、第１の半導体ベアチップ３のワイヤボンディングが行なわれる部分（ボンディングパッド11が配置されるチップの周辺領域）よりも内側の領域に収まる範囲内の大きさのものでなければならないという寸法上の制限がある。

【０００７】このため、図６に示す方法の場合、上記制限のために、設計の自由度が小さくなるという問題点があった。

【０００８】従って、本発明は、前記問題点を解消し、ハイブリッドＩＣに複数の半導体ベアチップを内蔵する場合に、適用範囲が広く、容易に実施できる高密度ベアチップの実装方法を提供することを目的とする。また、本発明は、設計の自由度の制限を解消し、高密度実装可能なハイブリッドＩＣを提供することを目的とする。

【０００９】

【課題を解決するための手段】前記目的を達成するため、本発明のハイブリッドＩＣの製造方法は、回路基板上に第１の半導体ベアチップを固着し、金属細線にて該回路基板と該第１の半導体ベアチップを回路接続し、次に、該第１の半導体ベアチップの露出した主面上に、後処理によって硬化する液状絶縁樹脂を、少なくとも該第１の半導体ベアチップ上の該金属細線の最大高さ部分まで覆うように吐出し、前記絶縁樹脂が未硬化状態のまま、第２の半導体ベアチップを前記絶縁樹脂上に置き、その後、金属細線にて前記回路基板と前記第２の半導体ベアチップを回路接続し、最終的に該第１、第２の半導体ベアチップと回路接続用の前記金属細線の全体を絶縁樹脂で封止して半導体チップを内蔵する、ことを特徴とするものである。

【００１０】本発明のハイブリッドＩＣの製造方法においては、好ましくは、前記絶縁樹脂を硬化させた後に、前記金属細線にて前記回路基板と前記第２の半導体ベアチップを回路接続することを特徴としている。

【００１１】また、本発明のハイブリッドＩＣの製造方法においては、前記回路基板と前記第１の半導体ベアチップを前記金属細線で回路接続した後、前記液状絶縁樹脂を吐出する前の段階で、絶縁体から成るスペーサを前記第１の半導体ベアチップ上に形成する工程が追加されたことを特徴としている。

【００１２】さらに、本発明のハイブリッドＩＣの製造方法においては、前記回路基板と半導体ベアチップを回路接続が、少なくとも前記第１の半導体ベアチップにおいては、絶縁樹脂被覆された金線のワイヤボンディングにより成されることを特徴とするものである。

【００１３】そして、本発明においては、回路基板上に複数の半導体ベアチップを積み重ねて成るハイブリッドＩＣの製造方法であって、第１層の半導体ベアチップを固着し、金属細線にて該回路基板と該第１の層の半導体ベアチップを回路接続し、前記第１の層の半導体ベアチップ上にさらに複数の半導体ベアチップを積み重ねる際に、すでに配置された下側の層の半導体ベアチップを金属細線にて該回路基板と回路接続した後に、前記下側の層の半導体ベアチップ上に絶縁樹脂を、少なくとも前記下側の層の半導体ベアチップの前記金属細線の最大高さ部分まで覆うように吐出し、前記絶縁樹脂上に上側の層の半導体ベアチップを置き、金属細線にて前記回路基板と前記の上側の層の半導体ベアチップを回路接続する、工程を順次繰り返して複数の半導体ベアチップを積層していき、最後に積層された複数の半導体ベアチップと回路接続用の前記金属細線の全体を絶縁樹脂で封止して半導体チップを内蔵するようにする、ことを特徴とするハイブリッドＩＣの製造方法を提供する。

【００１４】本発明のハイブリッドＩＣの製造方法においては、好ましくは、下側の層の半導体ベアチップ上に吐出された前記絶縁樹脂が未硬化の状態において前記上側の層の半導体ベアチップを該絶縁樹脂上に配置することを特徴としている。

【００１５】本発明のハイブリッドＩＣの製造方法において、好ましくは、前記回路基板と前記下側の層の半導体ベアチップを前記金属細線で回路接続した後、前記絶縁樹脂の吐出以前に、絶縁体から成るスペーサを前記下側の層の半導体ベアチップ上に形成することを特徴とするものである。さらに本発明においては、回路基板と下側の層の半導体ベアチップを回路接続が、少なくとも下側の層の半導体ベアチップの少なくとも一においては、絶縁樹脂被覆された金線のワイヤボンディングにより成されることを特徴とするものである。

【００１６】また、本発明は、回路基板上に固着され金属細線にて該回路基板と接続された第１の半導体ベアチップと、該第１の半導体ベアチップ上に少なくとも該第１の半導体ベアチップ上の該金属細線の最大高さ部分まで覆うように吐出された絶縁樹脂と、該絶縁樹脂上に置かれ、金属細線にて前記回路基板と回路接続した第２の

半導体ベアチップと、を備え、前記第１、第２の半導体ベアチップと該回路接続金属細線の全体を絶縁樹脂で封止して成るハイブリッドＩＣを提供する。

【００１７】本発明のハイブリッドＩＣにおいて、好ましくは、前記第１の半導体ベアチップ上に絶縁体から成るスペーサが配設されたことを特徴とするものである。

【００１８】

【作用】本発明によれば、回路基板上のワイヤボンディングされた半導体ベアチップ上にワイヤ高さよりも高く絶縁樹脂等による絶縁層を設け、その上に別の半導体ベアチップを配置したことにより、回路基板の片面側に複数の半導体ベアチップを搭載出来るため、回路基板の両面に置載する場合よりも遥かに製造が容易であり、また、積層される上下の半導体ベアチップについて寸法上の制約が存在しないため、上側の半導体ベアチップが下側の半導体ベアチップよりも平面寸法が所定のサイズ分小さくなければならないという前記従来例のような、設計の自由度に制約が課せられない。

【００１９】また、本発明によれば、積層される上下の半導体ベアチップについて上側の半導体ベアチップの裏面と下側の半導体ベアチップのボンディングワイヤとはその間に介挿される絶縁樹脂層により互いに電気的に絶縁される。そして、本発明においては上側の半導体ベアチップの裏面と下側の半導体ベアチップのボンディングワイヤとの隔離を確保して電気的絶縁を確実にするために、下側の半導体ベアチップにはスペーサが配置される。

【００２０】

【実施例】図面を参照して、本発明の実施例を以下に説明する。

【００２１】

【実施例１】図１及び図２は、本発明の一実施例のハイブリッドＩＣの半導体ベアチップ搭載部分の断面構造を工程順に示したものである。なお、単に図面作成の理由により製造工程は図１及び図２に亘って示されている。

【００２２】図１を参照して、所定の配線２が施された回路基板１上（図１（Ａ）参照）において、図１（Ｂ）に示すように、回路基板上１に接着剤４により第１半導体ベアチップ３を固着し、ワイヤボンディング法を用いてボンディングワイヤ５により第１半導体ベアチップ３のボンディングパッド11と回路基板１の所定の配線２とが互いに接続される。

【００２３】ボンディングワイヤ５は、通常、25μｍ～30μｍ径の金線が用いられる。

【００２４】次に、図１（Ｃ）に示すように、絶縁樹脂６を第１半導体ベアチップ３上に吐出する。絶縁樹脂６は、後処理によって硬化する液状樹脂とされ、好ましくは、熱硬化型のエポキシ樹脂等からなり、適当な粘度、チクソ性を有し、吐出してから硬化するまで大きくダレが発生しないものが用いられる。そして、絶縁樹脂６は

好ましくは、粘度100～200Ｐａ・ｓ、ＴＩ値（チクソ比）２～３のものが用いられる。

【００２５】図１（Ｃ）を参照して、絶縁樹脂６の吐出は、後にその上に載せる第２半導体ベアチップ７の下に絶縁樹脂６が充填されるように、また、先に施したボンディングワイヤ５よりも高くなるように行なう。

【００２６】例えば、第１半導体ベアチップ３のチップ面からのワイヤループ高さが200μｍであれば、第１半導体ベアチップ３のチップ面より300μｍ盛り上げて、上に載せる第２半導体ベアチップサイズよりも大きな範囲に塗布をする。

【００２７】次に、図２（Ｄ）に示すように、第２半導体ベアチップ７を、吐出した絶縁樹脂６上に載せ、絶縁樹脂６の硬化処理を行なう。

【００２８】絶縁樹脂６を未硬化のままで、第２半導体ベアチップ７を載せることにより、第２半導体ベアチップ７のチップ面の水平性が容易に確保出来る。

【００２９】また、第２半導体ベアチップ搭載時には、高さ制御を行なうことが下のボンディングワイヤ５との距離を確保する上で望ましい。

【００３０】この後、図２（Ｅ）に示すように、第２半導体ベアチップ７と回路基板１とをボンディングワイヤ５で接続し、最終的に第１、第２半導体ベアチップ３、７とボンディングワイヤ５の全てを封止樹脂８で封止する。

【００３１】第１半導体ベアチップ３上のボンディングワイヤ５と第２半導体ベアチップ７の裏面とは、電気的特性上、互いに絶縁されなければならないが、図１（Ｃ）の工程で説明したように、吐出される絶縁樹脂の性状と量、及び半導体ベアチップ搭載条件の調整を行なうことにより、絶縁樹脂６の層が、第１半導体ベアチップ３上のボンディングワイヤ５と第２半導体ベアチップ７の裏面との間に介挿され、これらは互いに隔離され電気的に絶縁される。

【００３２】

【実施例２】次に、本発明の別の実施例を以下に説明する。

【００３３】前記第１の実施例において、所望の性状の絶縁樹脂６を、電気特性や信頼性に与える影響等により採用することが困難である場合、または、製造工程上、最適な製造装置を用いることが出来ない場合等により、絶縁樹脂６の層を第１ベアチップ３上のボンディングワイヤ５と第２半導体ベアチップ７との間に安定して設けることが難しいときは、例えば、図３又は図４に示した別の製造方法が採られる。

【００３４】図３を参照して、本実施例においては、第１半導体ベアチップ３のワイヤボンディングを行なった後、絶縁樹脂６を吐出する前に、絶縁性の接着剤４により、第１半導体ベアチップ３上のボンディングワイヤ５との接触を確実に回避するに足る高さを有する絶縁性の

スペーサ９を第１半導体ベアチップ３上に固着させる。そして、スペーサ９を固着させた後に、前記第１の実施例と同様にして、絶縁樹脂６を吐出する。

【００３５】本実施例に従い、絶縁性のスペーサ９を第１半導体ベアチップ３上に設ける場合、絶縁樹脂６の粘度、チクソ性等の性状について、前記第１の実施例よりもその選択幅が緩和され、さらに、スペーサ９が介在することにより、第２半導体ベアチップ７を絶縁樹脂６上に置く際に絶縁樹脂６に加わる圧力の制御が簡易化され、第２半導体ベアチップ７の搭載時における高さ制御も容易化する。さらに、スペーサ９により第１半導体ベアチップ３の裏面とボンディングワイヤ５との隔離が確定・確保されるために、信頼性、及び歩留りの向上を図ることが可能とされる。

【００３６】

【実施例３】あるいは、本発明の別の実施例として、図４に示すように、下側の層となる第１半導体ベアチップ３のワイヤボンディングの際に、第１半導体ベアチップ３上のボンディングワイヤとして絶縁被覆が施された絶縁被覆ボンディングワイヤ10を用いる。絶縁被覆ボンディングワイヤとしては、例えば田中電子工業社製のＳＬワイヤや日本マイクロメタル社製のWタイプワイヤ等がある。

【００３７】以上、上記各実施例では、本発明を２段に積層された半導体ベアチップを例に説明したが、本発明に係るハイブリッドＩＣの製造方法は、半導体ベアチップを３段以上積み重ねる場合にも同様に用いることが出来る。

【００３８】そして、半導体ベアチップを３段以上積み重ねる場合に、下側の層の半導体ベアチップの上に吐出される絶縁樹脂が未硬化状態のまま、上側の層の半導体ベアチップを置き、絶縁樹脂が硬化した後に、回路基板とのワイヤボンディングを行なうようにしてもよいし、あるいは、絶縁樹脂の性状等によっては、絶縁樹脂が未硬化状態のまま、上側の層の半導体ベアチップと回路基板とのワイヤボンディングを行ない、各層の絶縁樹脂の硬化が同時的に進行するようにしてもよい。この場合、製造工程が短縮化される。

【００３９】以上、本発明を各種態様に即して説明したが、本発明は、上記実施例にのみ限定されるものではなく、本発明の原理に準ずる各種態様を含む。

【００４０】

【発明の効果】以上説明したように、本発明のハイブリッドＩＣの製造方法によれば、回路基板上のワイヤボンディングされた半導体ベアチップ上にワイヤ高さよりも高く絶縁樹脂等による絶縁層を設けて、その上に別の半導体ベアチップを配置したことにより、回路基板の片面側に複数の半導体ベアチップを内蔵出来るため、両面に置載する場合よりも製造が容易とされ、また、上下の半導体ベアチップの寸法上の制約が存在しないため、設計の自由度が拡張し、適用範囲が拡大すると共に、複数段の高密度実装を容易化し且つ歩留りを向上するという効果を有する。

【００４１】本発明によれば、半導体ベアチップの裏面と下層の半導体ベアチップのボンディングワイヤとはその間に介挿される絶縁樹脂層により互いに電気的に確実に絶縁されている。そして、本発明によれば、吐出された絶縁樹脂が未硬化状態のうちにその上に半導体ベアチップが置かれるために、チップ面の水平性が容易に確保される。

【００４２】また、本発明のハイブリッドＩＣの製造方法によれば、例えば製造上の理由等により、半導体ベアチップの裏面と下層の半導体ベアチップのボンディングワイヤとの絶縁樹脂層による確実な絶縁が困難とされる場合、絶縁樹脂の吐出以前に、絶縁体から成るスペーサを下層半導体ベアチップ上に形成することにより、回路基板の片面側に複数の半導体ベアチップを内蔵出来るため、両面に置載する場合よりも製造が容易であり、また、上下の半導体ベアチップの寸法上の制約が存在しないため、設計の自由度が拡がり、適用の範囲が大きく出来るという効果を有する。さらにスペーサを設けるようにした場合、下層半導体ベアチップと上層半導体ベアチップ内の高さ制御が容易にされるとともに、電気的絶縁層を確実なものとする。

【００４３】さらに、本発明のハイブリッドＩＣの製造方法によれば、下層側の半導体ベアチップのボンディングワイヤとして、絶縁被覆ボンディングワイヤを用いることによっても、電気的絶縁層を確保するという効果を有する。

【００４４】そして、本発明のハイブリッドＩＣの構成によれば、多段に高密度実装する場合において、従来存在していた寸法上の設計の自由度の制約が解消されており、適用可能性が拡大されると共に、各層とボンディングワイヤの電気的絶縁が確保され、製造工程を容易化し、歩留りを向上させる。

【図面の簡単な説明】

【図１】（Ａ）～（Ｃ）は、本発明の一実施例の製造工程を順に示した断面図である。

【図２】（Ｄ）～（Ｅ）は、本発明の一実施例の製造工程（図１に後続する工程）を順に示した断面図である

【図３】本発明の第２実施例を示す断面図である。

【図４】本発明の第２実施例を示す断面図である。

【図５】従来例の構成を示す断面図である。

【図６】別の従来例の構成を示す断面図である。

【符号の説明】

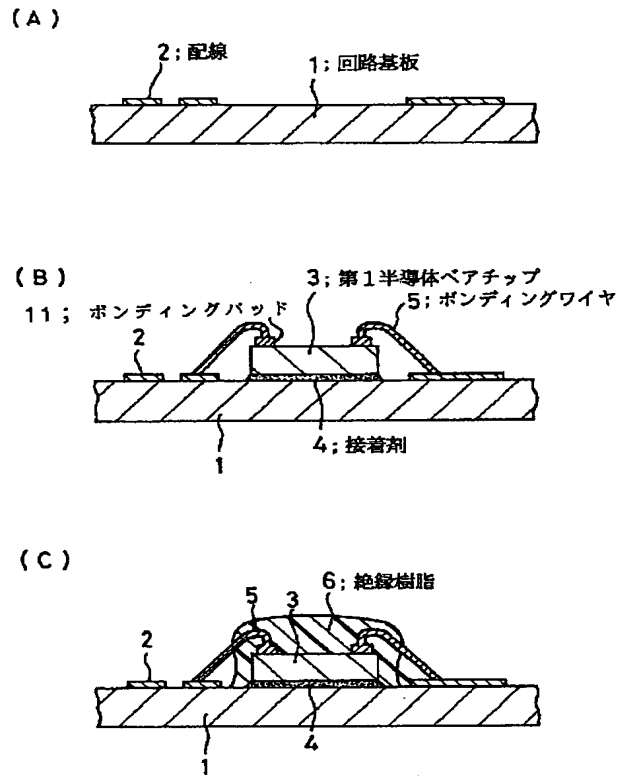
1　回路基板
3　第１半導体ベアチップ
5　ボンディングワイヤ
6　絶縁樹脂
7　第２半導体ベアチップ

9　スペーサ

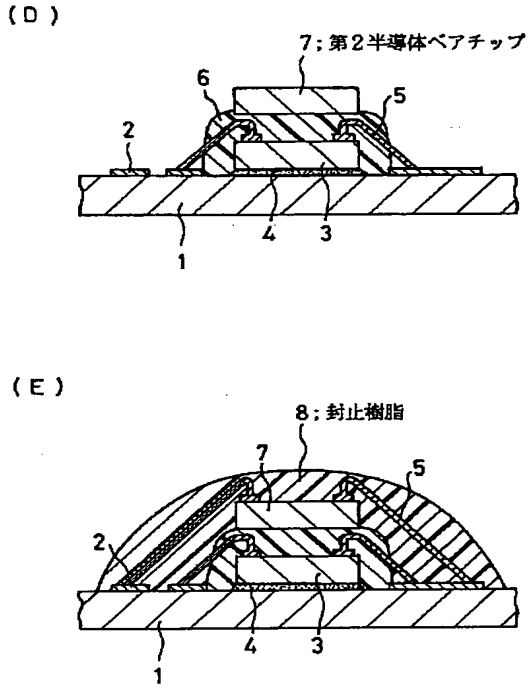
10　絶縁被覆ボンディングワイヤ

11　ボンディングパッド

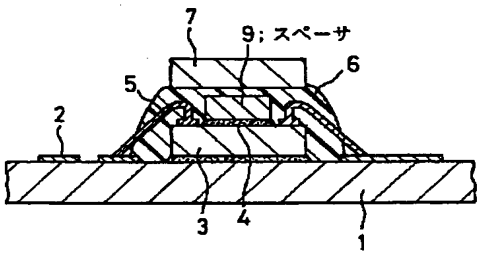
【図１】



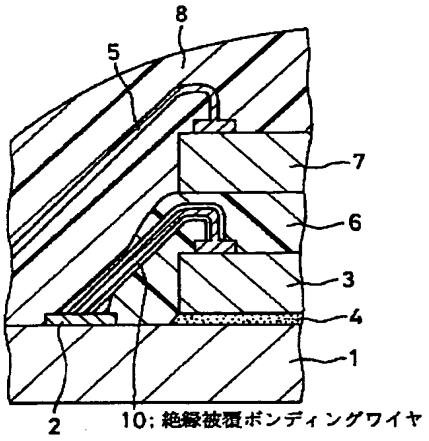
【図２】



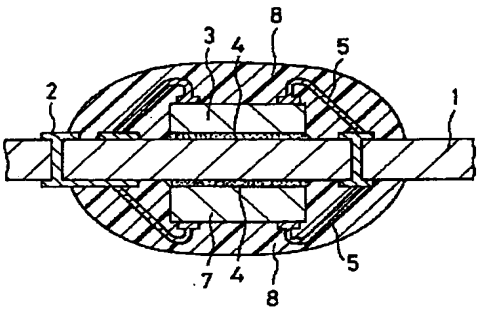
【図３】



【図４】



【図５】



【図６】